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SSI 78P7200
DS-3/E3/STS-1 Line Interface with Receive Equalizer

September 1995

DESCRIPTION

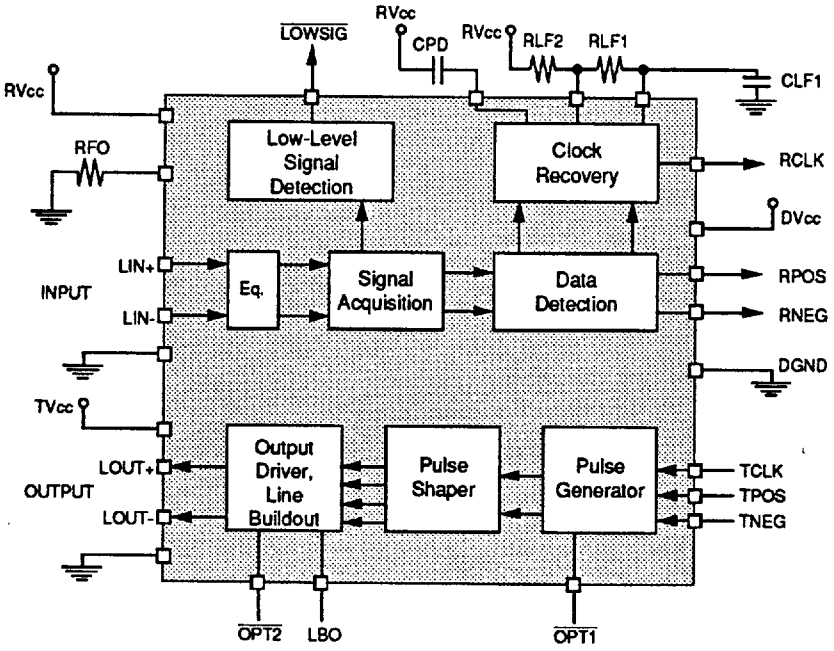
The SSI 78P7200 is a line interface transceiver IC intended for STS-1 (51.84 Mbit/s), DS-3 (44.736 Mbit/s) and E3 (34.368 Mbit/s) applications. The receiver has a very wide dynamic range and is designed to accept HDB3 or B3ZS-encoded Alternate-Mark Inversion (AMI) inputs; it provides CMOS logic level clock, positive data, negative data and low-level signal detector outputs. An on-chip equalizer improves the intersymbol interference tolerance on the receive path. The transmitter converts CMOS logic level clock, positive data and negative data input signals into AMI pulses of the appropriate shape for transmission. A line buildout (LBO) equalizer may be selected to shape the outgoing pulses for shorter line lengths. The SSI 78P7200 requires a single 5 volt supply and is available in DIP and surface mount packages.

The 78P7200 works in either rate of STS-1, DS-3 or E3 by simple external components modification.

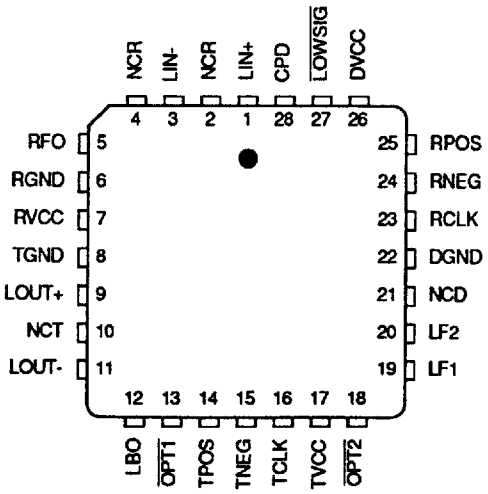
FEATURES

- **Single chip transmit and receive interface for STS-1 (51.84 Mbit/s), E3 (34.368 Mbit/s) or DS-3 (44.736 Mbit/s) applications**
- **On-chip Receive Equalizer**
- **Unique clock recovery circuit, requires no crystals, tuned components or external clock**
- **Selectable transmit line buildout (LBO) to accommodate shorter line lengths**
- **Compliant with ANSI T1.102-1993, Bellcore TR-NWT-000499 and GR-253-CORE, ITU-T G.703 and G.823_1991**
- **Low-level input signal indication**
- **Available in DIP or surface mount packages**
- **-40°C to +85°C operating range**
- **Pin-compatible replacement for SSI 78P236, 78P2361 and 78P2362**

BLOCK DIAGRAM



PIN DIAGRAM



28-Pin PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 78P7200 is a single chip line interface IC designed to work with a 51.84 Mbit/s STS-1, 44.736 Mbit/s DS-3 or 34.368 Mbit/s E3 signal. The receiver recovers clock, positive data and negative data from an Alternate Mark Inversion (AMI) signal. The input signal should be B3ZS or HDB3 coded.

The transmitter accepts CMOS level logical clock, positive data and negative data and converts them to the AMI signal to drive a 75Ω coaxial cable. Programmable internal Line Buildout (LBO) circuitry eliminates the need for external LBO networks. When the option pins are properly selected, the shape of the transmitted signal through any cable length of 0 to 450 feet complies with the published templates of ANSI T1.102, ITU-T G.703, Bellcore TR-NWT-000499 and GR-253-CORE. The SSI 78P7200 is designed to work with a B3ZS or HDB3 coded signal. The B3ZS or HDB3 encoding and decoding functions are normally included in the framer ICs or can easily be implemented in a PAL.

RECEIVER

The receiver input is normally transformer-coupled to the AMI signal. The inputs to the IC are internally referenced to RVCC. Since the input impedance of the SSI 78P7200 is high, the AMI line must be terminated in 75Ω. The input signal to the SSI 78P7200 must be limited to a maximum of three consecutive zeros using a coding scheme such as B3ZS or HDB3.

The AMI signal first enters a fixed equalizer which is designed to overcome the intersymbol interference caused by long cable lengths and crosstalk. This fixed equalizer is optimized for DS-3 application and its effect should be compensated by an external filter circuit similar to Fig. 1, for all square shaped signals such as DS3-high or 34 Mbit/s E3. The signal is then input to a variable gain differential amplifier whose output is maintained at a constant voltage level regardless of the input voltage level. The gain of this amplifier is adjusted by detecting the peak of the signal and comparing it to a fixed reference.

The output of the variable gain amplifier is compared to a threshold value which is a fixed percentage of the signal peak. In this way, even though the input signal amplitude may fall below the minimum value that can be regulated by the variable gain circuit, the proper detection threshold is maintained.

Outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase locked loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator.

This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high precision and/or adjustable oscillator or tuned circuits.

The response characteristic for the phase locked loop is established by external filter components, RLF1, RLF2 and CLF1. The values of these components are specified such that the bandwidth of the phase locked loop is greater than 200 kHz.

The jitter tolerance of the SSI 78P7200 exceeds the requirements of TR-NWT-000499 for Category II equipment for DS-3 rate and exceeds the requirements of ITU-T G.823 for E3 rate. The jitter transfer function is maximally flat so the IC doesn't add any significant jitter to the system.

Figure 2 shows the recovered clock (RCLK), positive data (RPOS) and negative data (RNEG) signals timing. The data is valid on the rising edge of the clock. The minimum setup and hold times allow easy interface to framer circuits. These signals are CMOS-level outputs.

Should the input signal fall below a minimum value, the $\overline{\text{LOWSIG}}$ pin goes active low. A time delay is provided before this output is active so that transient interruptions do not cause false indications. This signal should be used as one of many indications to the cable disconnect; the framer device should count the number of zeros to declare the loss of signal. The RPOS and RNEG signals generate random data following a silence period. The framer device should ignore RPOS and RNEG data if the $\overline{\text{LOWSIG}}$ pin is active low.

TRANSMITTER

The transmitter accepts unipolar CMOS level logical clock (TCLK), positive data (TPOS) and negative data (TNEG) signals and generates high current drive pulses on the LOUT+ and LOUT- pins. When properly connected to a center tapped transformer, an AMI pulse is generated which can drive a 75Ω coaxial cable.

Figure 3 shows the timing for the transmitter logic signals. The output pulse width is internally set and is not sensitive to input clock (TCLK) pulse width.

When a recommended transformer is used and option pins are properly set, the transmitted pulse shape at the end of a 75Ω terminated cable of 0 to 450 feet will fit the template for DSX3 pulse published in ANSI T1.102-1993, Bellcore TR-NWT-000499 documents.

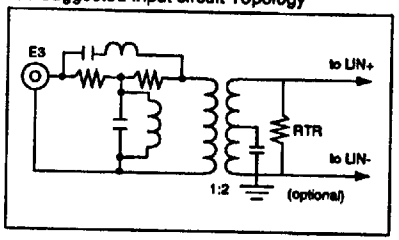
For 51.84 Mbit/s STS-1 application the transmitted pulse for a short cable meets the requirements of Bellcore GR-253-CORE. For 34 Mbit/s E3 application, the transmitted pulse for a short cable meets the requirements of ITU-T G.703 when both LBO and $\overline{\text{OPT1}}$ pins are set LOW.

The SSI 78P7200 incorporates a selectable Line Buildout (LBO) pulse shaper in the transmitter path. For STS-1 and DS-3 applications, the LBO pin should be set HIGH if the cable is shorter than 225 feet and set LOW for longer cable lengths. For E3 application, LBO pin should be set LOW regardless of cable length.

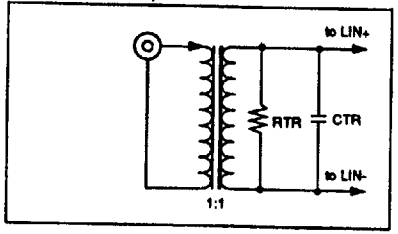
The $\overline{\text{OPT1}}$ pin is set HIGH for normal DS-3 and STS-1 operation. Setting the $\overline{\text{OPT1}}$ pin to LOW increases the transmitter power. The $\overline{\text{OPT1}}$ pin should be set LOW for E3 applications.

The $\overline{\text{OPT2}}$ pin should be set HIGH for normal operation. Setting the $\overline{\text{OPT2}}$ pin to LOW disables the transmitter drivers and reduces the power consumption of the circuit by approximately 125 mW.

E3 Suggested Input circuit Topology



STS-1 or DS-3 Input circuit



Note: Only one of the two input circuits is needed

Note: Refer to 78P7200_E3 application note for details of E3 input circuit

Note: NC pins should be tied to the ground pin indicated by the trailing letter.

FIGURE 1: Functional Diagram

PIN DESCRIPTION

RECEIVER

NAME	TYPE	DESCRIPTION
LIN+, LIN-	I	Differential inputs, transformer-coupled from line.
RPOS	O	Unipolar receiver output, active as result of positive pulse at inputs.
RNEG	O	Unipolar receiver output, active as result of negative pulse at inputs.
RCLK	O	Clock pulses recovered from line data.
$\overline{\text{LOWSIG}}$	O	Low signal logic output indicating that input signal is less than threshold value.

TRANSMITTER

TPOS	I	Unipolar transmitter data input, active high.
TNEG	I	Unipolar transmitter data input, active high.
TCLK	I	Transmitter clock input, active high.
LOUT+	O	Output to transformer for positive data pulses.
LOUT-	O	Output to transformer for negative data pulses.
LBO	I	Transmitter line buildout control. Set low for all E3 or for DS-3/STS-1 cable of 225' or longer. Set high for short DS-3/ STS-1 cable.
$\overline{\text{OPT1}}$	I	Transmit option 1. Selects faster output pulse transition time and higher amplitude when low. Set high for normal DS-3/STS-1 and set low for E3.
$\overline{\text{OPT2}}$	I	Transmit option 2. Disables output driver and reduces output bias current when low. Set high for normal transmit operation.

EXTERNAL COMPONENT CONNECTION

RFO	I	Resistor connected to RGND to provide basic center frequency of receiver phase locked loop oscillator.
LF1, LF2	-	Resistor-capacitor loop filter network to establish bandwidth of phase locked loop.
CPD	-	Capacitor to RVcc that is connected to peak detector node to reduce signal-dependent ripple on that node.

POWER

TVcc	-	5V power supply for transmit circuits.
RVcc	-	5V power supply for receive circuits.
DVcc	-	5V power supply for receive logic circuits.
TGND	-	Ground return for transmit circuits.
RGND	-	Ground return for receive circuits.
DGND	-	Ground return for receive logic circuits.
NCR	-	No connect, Tie to Receiver Ground (RGND).
NCT	-	No connect, Tie to Transmitter Ground (TGND).
NCD	-	No connect, Tie to Digital Ground.

ELECTRICAL SPECIFICATIONS

(TA = -40°C to 85°C, Vcc = 5V ±5%, unless otherwise noted.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value. Operation above absolute maximum ratings may permanently damage the device.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Positive 5V supply: TVcc, RVcc, DVcc	6V
Storage Temperature	-65 to 150°C
Soldering Temperature (10 sec.)	260 °C
Ambient Operating Temperature, TA	-40 to +85°C
Pin Ratings: LOUT+, LOUT-	Vcc -2 to Vcc +2V
LIN+, LIN-, TPOS, TNEG, TCLK, LBO, RFO, LF2, LF1, $\overline{OPT1}$, $\overline{OPT2}$ Pins	-0.3 to Vcc +0.3V
RPOS, RNEG, RCLK, $\overline{LOWSIG}$ Pins	-0.3 to Vcc +0.3V or +12 mA

SUPPLY CURRENTS AND POWER

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current	ICC	Outputs unloaded, normal operation, transmit and receive all 1's pattern		155	190	mA
Power Dissipation	P	Outputs unloaded, TA = 85°C			0.93	W

EXTERNAL COMPONENTS (Common to STS-1/DS3/E3, nominal value)

Loop filter resistor	RLF1	1% tolerance		6.04		kΩ
Loop filter resistor	RLF2	1%		100		kΩ
Loop filter capacitor	CLF1	5%		0.22		µF
Peak detector capacitor	CPD	10%		0.022		µF

EXTERNAL COMPONENTS (Dependent on speed, nominal Value)

			STS-1	DS-3	E3	
Loop center frequency resistor	RFO	1% tolerance	4.53	5.23	6.81	kΩ
Transmit termination capacitor	CTT	5% (Note 1)	10	10	3	pF
Transmit termination resistor	RTT	1%	301	301	604	Ω
Receive termination resistor	RTR	1%	75	75	Note 2	Ω
Receive termination capacitor	CTR	5%	5	5		pF
Receive Transformer Turns Ratio	T1	3%	1:1	1:1	Note 2	

Note 1: C_{TT} value depends on the PC board design. Nominal values are selected for SSI 78P7200 Demo Board.
Note 2: Refer to 78P7200_E3 application note for details.

DIGITAL INPUTS AND OUTPUTS

(CMOS-compatible pins: $\overline{\text{LOWSIG}}$, RPOS, RNEG, RCLK, TPOS, TNEG, TCLK, LBO, $\overline{\text{OPT1}}$.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Input low voltage	VIL		-0.3		1.5	V
Input high voltage	VIH		3.5		Vcc +0.3	V
Input low current	IIL	VIL = 1.5V	-5		5	µA
Input high current	IIH	VIH = 3.5V	-5		5	µA
Output low voltage	VOL	IOL = 0.1 mA			0.4	V
Output high voltage	VOH	IOH = -0.1 mA	4			V

$\overline{\text{OPT2}}$ CHARACTERISTICS

Input low voltage	VIL	IIL = 0.4 mA			0.5	V
Input high voltage	VIH		2			V

RECEIVER

All of the measurements for the receiver are made with the following conditions unless otherwise stated:

1. The input signal is transformer coupled as shown in Figure 1.
2. RFO = 5.23 kΩ for DS-3, 6.81 kΩ for E3 and 4.53 kΩ for STS-1.

Input signal voltage	VIN	Input AC-Coupled CPD = 0.022 µF	±0.045		±1.2	V
		CPD not used	±0.090		±1.2	V
Input Resistance	RIN	Input at device's common mode voltage	15	20	30	kΩ
Receive data detection threshold	VDTH	Relative to peak amplitude for 22.37/17.18/25.92 MHz sinusoidal input		50		%
Receive data low signal threshold	VLOW		±20		±50	mV
Receive data low signal delay	TLOW	CPD = 0.022 µF		500		µs
		CPD not used VIN(max) = ±250 mV	0.5		3	µs
Receive clock period	TRCF	DS-3		22.35		ns
		STS-1		19.29		ns
		E3		29.1		ns

RECEIVER (continued)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
Receive clock pulse width TRC		DS-3		12.24		ns
		STS-1		9.65		ns
		E3		14.55		ns
Receive clock positive transition time TRCPT	C_L = 15 pF			4.5	6	ns
Receive clock negative transition time TRCNT	C_L = 15 pF			4.5	6	ns
Positive or negative receive data pulse width TRDP/TRDN		DS-3		22.35		ns
		STS-1		19.29		ns
		E3		29.1		ns
Receive data set-up time TRDPS/TRDNS		DS-3	5	11.18	13.7	ns
		STS-1		9.65		ns
		E3	5	14.55		ns
Receive data hold time TRDPH/TRDNH		DS-3	5	11.18	13.7	ns
		STS-1		9.65		ns
		E3	5	14.55		ns
Receive input jitter tolerance high frequency (Note 1)	60 - 300 kHz VIN (min) = ±45 mV	DS-3 STS-1	0.3			UIPP
	10 - 800 kHz VIN (min) = ±45 mV	E3	0.15			UIPP
	10 - 800 kHz VIN (min) = ±90 mV	E3	0.20			UIPP
Receive input jitter tolerance low frequency (Note 1)	10 Hz to 2.3 kHz	STS-1, DS-3	10			UIPP
	100 Hz to 10 kHz	E3	10			UIPP
Clock Recovery Phase Detector Gain KD	All 1's data pattern, KD = 0.418/RFO	DS-3	72	80	88	µA/Rad
		STS-1		92		µA/Rad
		E3		62		µA/Rad
Clock Recovery Phase Locked Oscillator Gain KO			12	14.5	17	Mrad/ sec. -Volt

Note 1: UI (Unit Interval) defined as 22.35 ns for DS-3, 29.1 ns for E3 and 19.29 ns for STS-1.

TRANSMITTER

All of the measurements for the transmitter are made with the following conditions unless otherwise stated:

1. Transmit pulse characteristics are obtained using a line transformer which has the characteristics, similar to Pulse Engineering PE-65969, Mini circuit T4-1, Valor PT5045.
2. The circuit is connected as in Figure 1.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Transmit clock repetition TTCF	DS-3		22.35		ns
	STS-1		19.29		ns
	E3		29.1		ns
Transmit clock pulse width TTC	DS-3		11.18		ns
	STS-1		9.65		ns
	E3		14.55		ns
Transmit clock negative transition time TTCNT			4.5	6	ns
Transmit clock positive transition time TTCPT			4.5	6	ns
Transmit data set-up time TTPDS	DS-3	3.5	11.18		ns
	STS-1	3.5	9.65		ns
TTNDS	E3	3.5	14.55		ns
Transmit data hold time TTPDH	DS-3	3.5	11.18		ns
	STS-1	3.5	9.65		ns
TTNDH	E3	3.5	14.55		ns
Transmit positive line pulse width TTPL	Measured at transformer, LBO = High DS-3	10.62	11.18	12	ns
	LBO = High STS-1		9.65		ns
	LBO = Low E3		14.5		ns
Transmit negative line pulse width TTNL	Measured at transformer, LBO = High DS-3	10.62	11.18	12	ns
	LBO = High STS-1		9.65		ns
	LBO = Low E3		14.5		ns
Transmit line pulse waveshape	See Note 1 for DS-3 See Note 2 for E3 See Note 3 for STS-1				

Note 1: Characteristics are in accordance with ANSI T1.102 - 1993 Table 4 and Figure 4.
Note 2: Characteristics are in accordance with ITU-T G.703 - 1991 Figure 17.
Note 3: Characteristics are in accordance with ANSI T1.102 - 1993 Figure A.1.

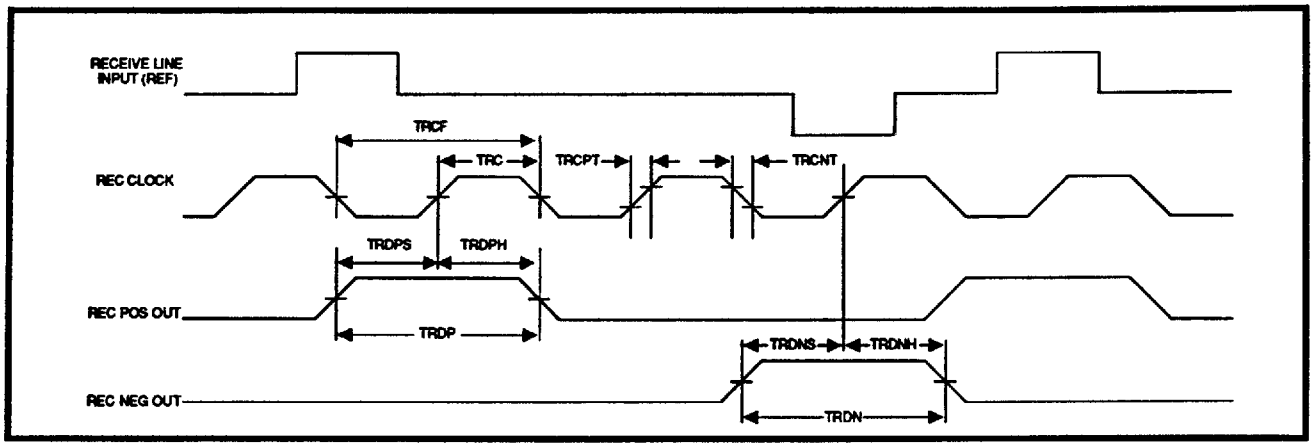


FIGURE 2: Receive Waveforms

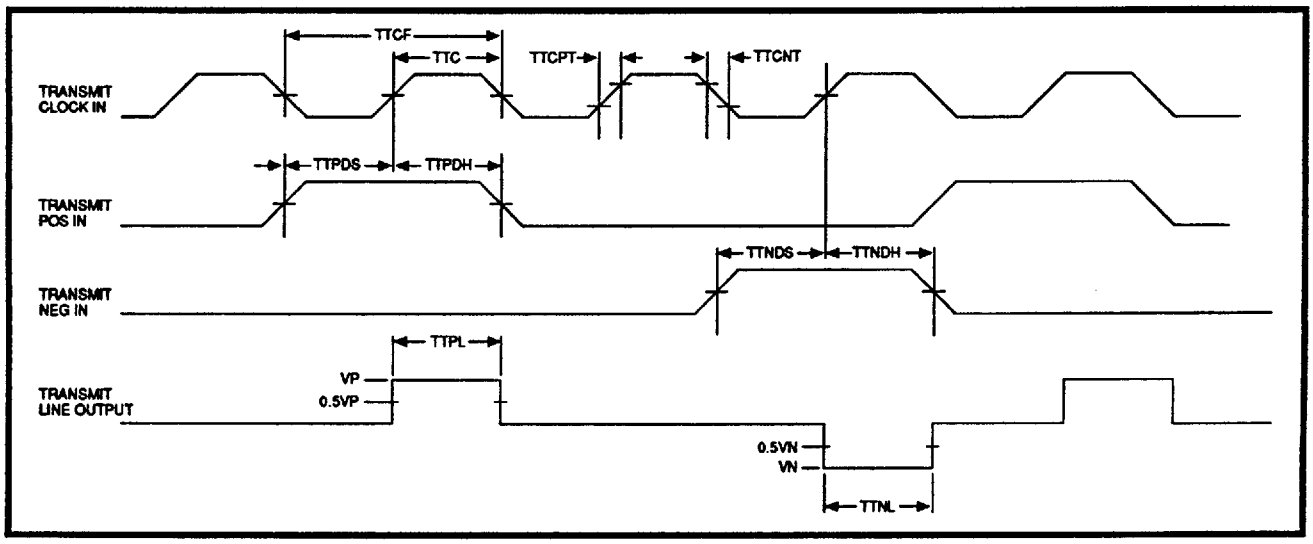
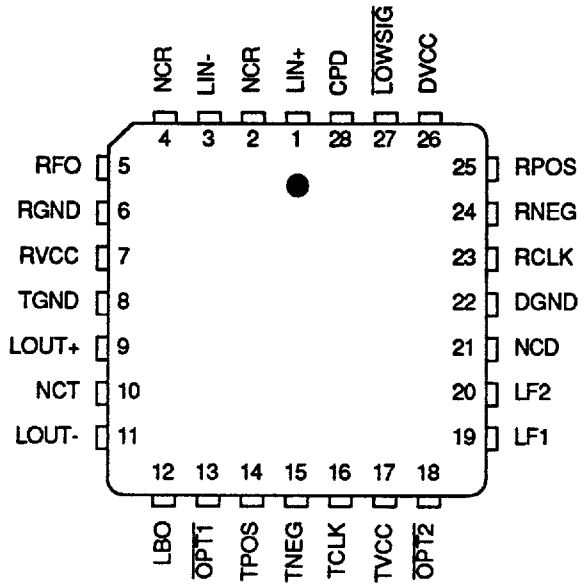


FIGURE 3: Transmit Waveforms

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 78P7200, DS-3/E3/STS-1 Line Interface 28-pin		
Standard Width Plastic DIP (600 mil)	78P7200-IP	78P7200-IP
Surface Mount 28-pin PLCC	78P7200-IH	78P7200-IH

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680-7022, (714) 573-6000, FAX (714) 573-6914

